DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

a second interlayer insulating film, the entire part of the second interlayer insulating film having a tensile stress, provided on [~~so as to directly cover~~] the first interconnect [~~and the first interlayer insulating film~~]; and

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film[~~; and~~

~~a passivation layer provided so as to cover the second interconnect, wherein the second interconnect provided on the second interlayer insulating film so as to cover at least a part of the capacitor~~].

32. (Currently amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate [~~having an integrated circuit thereon~~] and including a lower electrode, a [~~dielectric~~] feroelectric film, and an upper electrode;

a first interlayer insulating film provided so as to [~~directly~~] cover the capacitor, the first interlayer insulating film having a tensile stress;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to [~~the integrated circuit and~~] the capacitor through a first contact hole formed in the first interlayer insulating film;

DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

a second interlayer insulating film, the entire part of the second interlayer insulating film having a tensile stress, provided on [~~so as to directly cover~~] the first interconnect [~~and the first interlayer insulating film~~]; and

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film[; ~~and~~

~~a passivation layer provided so as to cover the second interconnect~~], wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor.

35. (New) The semiconductor device of claim 1, further comprising a passivation layer provided so as to cover the second interconnect.

Remarks

I. **CLAIM 1, 6, 10, 29 AND 32 ARE NOT UNPATENTABLE OVER APPLICANT'S SPECIFICATION IN VIEW OF WHITE, JR ET AL.**

Claim 1, 6, 10, 29 and 32 stand rejected under 35 U.S.C. § 103(a) over Applicant's specification in view of White, Jr et al.. This rejection is respectfully traversed for the following reasons.

DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

White, Jr et al filed on November 3, 1997. On the contrary, our application has a priority based on the corresponding Japanese application dated June 24, 1997, that is prior to the filing date of White, Jr et al.. All independent claims are disclosed in the Japanese priority document. Thus, White, Jr, et al. is not a prior art reference and any of claims are not unpatentable under 35 U.S.C. § 103(a) over Applicant's specification in view of White, Jr et al.

II. **CLAIM 1, 7-9, and 29- 32 ARE NOT UNPATENTABLE OVER APPLICANT'S SPECIFICATION IN VIEW OF MATSUKI ET AL.**

Claim 1, 7-9 and 29-32 stand rejected under 35 U.S.C. § 103(a) over Applicant's specification in view of Matsuki et al.. This rejection is respectfully traversed for the following reasons.

Among the all pending claims, only claim 1 and 32 are independent claims. As recited by each of the pending independent claims, the present invention recites that the "a second interlayer insulating film, the entire part of the second interlayer insulating film **having a tensile stress**, **provided on the first interconnect** ". That is to say, in our invention "a second interlayer insulating film" insulate a second interconnect from a first inter connect. On the contrary, "the second insulating layers of Matsuki" **are not provided on the first interconnect**, but provided on the first insulating film. Matsuki's

(1)

DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

insulating layers have two layers structure, but both insulate a first interconnect from a capacitor. Thus "the second insulating layers of Matsuki" are not "a second interlayer insulating film" recited in each independent claim. Further, in Applicant's admitted prior art, a second interlayer insulating, which is provided on the first interconnect, has **a compressive stress**, not a tensile stress. That is to say, both Matsuki and Applicant's admitted prior art are completely silent to "**a second interlayer insulating film, the entire part of the second interlayer insulating film having a tensile stress, provided on the first interconnect**."

Accordingly, as each and every claim limitation must be disclosed or suggested by the prior art reference in order to establish a *prima facie* case of obviousness **(see, M.P.E.P. § 2143.03)**, and both Applicant's admitted prior art and Matsuki el al fail to do so for at least the foregoing reasons, it its respectfully submitted that each independent claim is patentable over Applicant's specification in view of Matsuki et al.

Further, one of the objects of our invention is to solve the problem that is unique to the multilayer interconnect structure. That is to say, in the multilayer interconnect structure, the second interlayer insulating film requires sufficient planarization in order to process the second interconnection layer into desired shape, to do so the second interlayer insulating film needs sufficient thickness. But a thicker layer results in a stronger stress, so compressive stress of the second interlayer insulating film likely to cause degradation of capacitance (polarization). In order to solve the problem, a

DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

second interlayer insulating film, which is provided on the first interconnect, has a tensile stress, because the tensile stress suppresses degradation of capacitance in contrast to a compressive stress (see page 32 line 1-7 of Applicant's specification). On the contrary, Matsuki et al use two layered structure as one insulating film, one layer Is sputtered silicon oxide film which has a compressive stress and another layer is TEOS film which has a tensile stress in order to **cancel or mitigate the warp of the substrate generated by the suputtering** (see colum 6 line 54-59 of Matsuki). Our invention based on the recognition **that tensile stress suppresses degradation of capacitance in contrast to compressive stress** (see page 32 line 1-7 of Applicant's specification). Matsuki et al disclose neither the multilayer interconnect structure nor the recognition of tensile stress. So there is no motivation or suggestion that combine the Applicant's specification to Matsuki et al.

III. CLAIM 4 is NOT UNPATENTABLE OVER APPLICANT'S SPECIFICATION IN VIEW OF WHITE, JR ET AL, AND FURTHER IN VIEW OF MATSUURA ET AL.

Claim 4 stands rejected under 35 U.S.C. § 103(a) over Applicant's specification in view of White, Jr et al, and further in view of Matsuura et al.. This rejection is respectfully traversed for the following reasons.

White, Jr et al filed on November 3, 1997. On the contrary, our application has a priority based on the corresponding Japanese application dated June 24, 1997, that is

DRAFT - FOR EXAMINER REVIEW ONLY
NOT FOR FILING

prior to the filing date of White, Jr et al.. All independent claims are disclosed in the Japanese priority document. Thus, White, Jr, et al. is not a prior art reference and any of claims are not unpatentable under 35 U.S.C. § 103(a) over Applicant's specification in view of White, Jr et al.